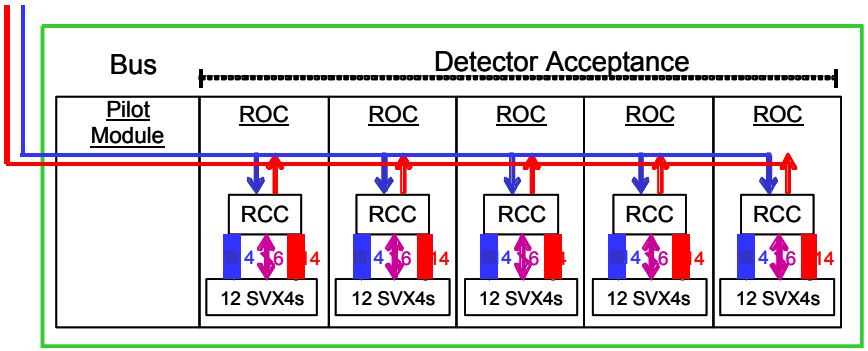
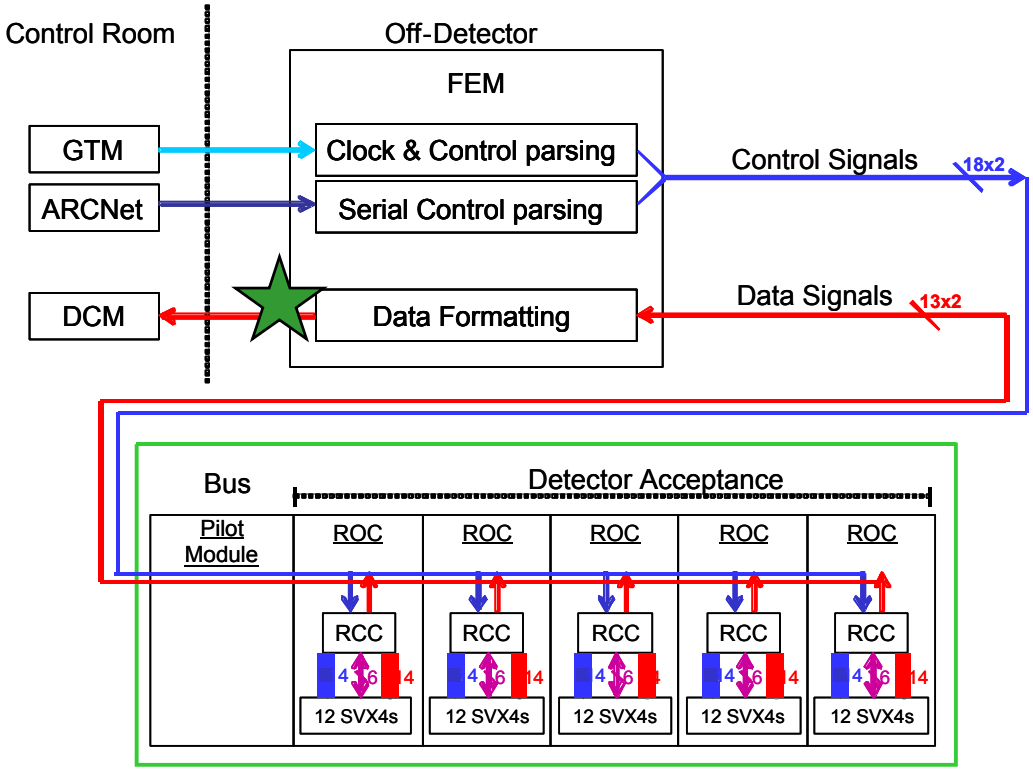
# Strip-pilot Data Output: LVDS or Optical?



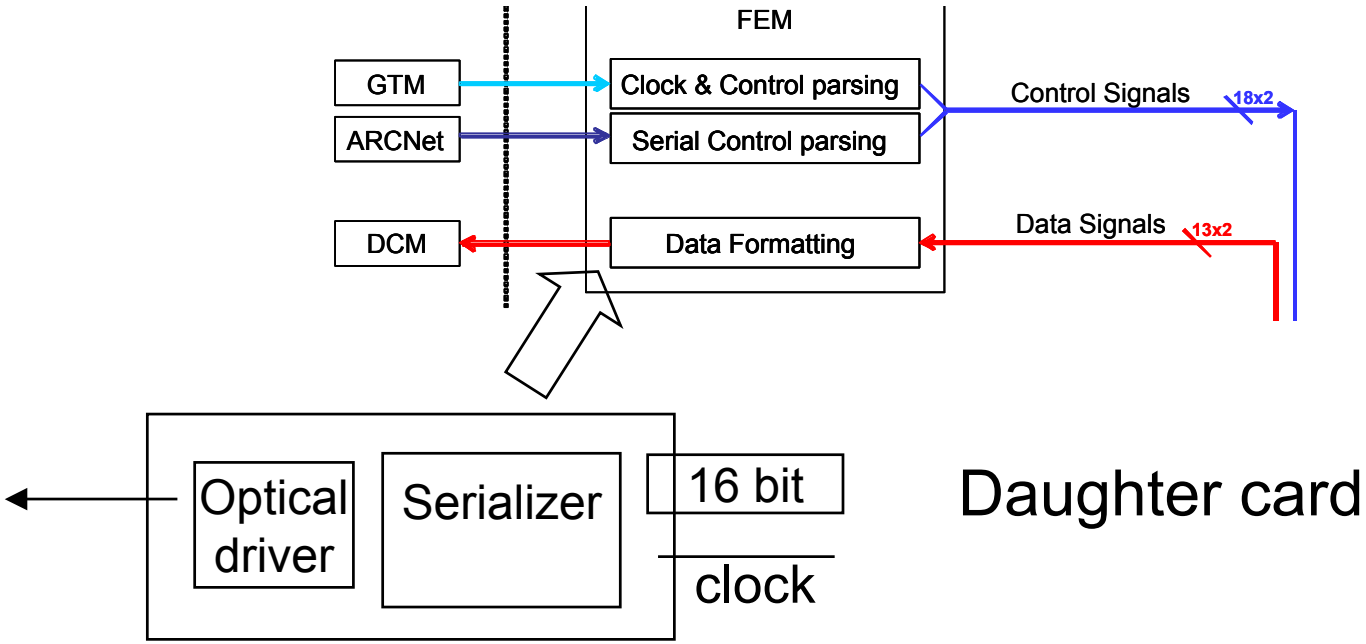

- LVDS pros
  - less size, power, complexity on pilot
    - » (LVDS driver) vs (serializer + optical driver)
  - LVDS drivers rad-tolerant to 50kRad
    - » Serializers needed for optical solution
      - ◆unknown rad-tolerance
- LVDS cons
  - Ground loop?

# Optical Daughter Card




- We started work on daughter card that could either
  - Transmit data from FEM to DCM, or from pilot to FEM
  - Make it general for use in all PHENIX upgrades

# Optical Daughter Card




- In FEM, less constraints size, rad-hardness
- Serializer options
  - Depends on encoding 8B/10B or CIMT, Chi?
  - TLK1501 (8B/10B) , GLINK 3.3V (CIMT)
- Optical drivers, many, Agilent HFBR-5912

# Schedule

- Design complete end of September
- Test board back by mid-October
- Goal
  - complete this simple task,
  - work with Vince/Chi to see if we can help on other parts of the system

# backup

# Strip Requirements (TVC March 04)

- Two readout cards (ROC) per sensor
  - Each ROC has 6 SVX4 + FPGA / ASIC
  - 8 ROCs per ladder
  - 48 svx4 per ladder
- Volume per SVX4
  - Each hit = 16 bit word
  - 1 header
  - Total words/svx4 = 1+(num hits) = 1+(occ*128)
- Volume per ladder
  - Total words/ladder = 48+(occ*6144)
- Time = (48+(occ*6144))/40 MHz
  - < 40 microsec if occ < 25%
- Serialize each 16 bit word at 40 MHz